IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 5, Issue 1, January 2016

An Approach for using Token Memory in Parallel Processing

Buddh Bhagwan Sahu[1], Prof. Rajesh Tiwari [2]

M.E. Computer Science & Engineering Dept., Shankaracharya Group of Institutions, Bhilai (C.G.), India[1]

Associate Prof., Computer Science & Engineering Dept., Shankaracharya Group of Institutions, Bhilai (C.G.), India [2]

Abstract: A parallel computer (or multiple processor system) is a collection of communicating processing elements (processors) that cooperate to solve large computational problems fast by dividing such problems into parallel tasks, exploiting Thread-Level Parallelism (TLP).The major issues involved in parallel processing are the concurrency and communication characteristics of parallel algorithms for a given computational problem, The number of processing elements (PEs), computing power of each element and amount/organization of physical memory used, how the processing elements cooperate and communicate and how data is shared/transmitted between processors. The major approach of the work is to propose a token memory architecture to reduce the load on CPU parallel processing .During peak period the heavy tasks will be transferred to this token memory so as to reduce load on CPU.

Keywords: CPU (Central Processing Unit), Token memory, Parallel Processing, Token Memory.

I. INTRODUCTION

This document is a template. An electronic copy can be Parallel processing is a method of simultaneously breaking up and running program tasks on multiple microprocessors, thereby reducing processing time. Parallel processing may be accomplished via a computer with two or more processors or via a computer network. Parallel processing is also called parallel computing. The major advantages of parallel processing include:

Save time and/or money: In theory, throwing more resources at a task will shorten it's time to completion, with potential cost savings. Parallel computers can be built from cheap, commodity components.

Solve Larger / More Complex Problems: Many problems are so large and/or complex that it is impractical or impossible to solve them on a single computer, especially given limited computer memory.

Provide Concurrency: A single compute resource can only do one thing at a time. Multiple compute resources can do many things simultaneously.

Take Advantage Of Non-Local Resources: Using computer resources on a wide area network, or even the Internet when local compute resources are scarce or insufficient.

Make Better Use Of Underlying Parallel Hardware: Modern computers, even laptops, are parallel in architecture with multiple processors/cores. Parallel software is specifically intended for parallel hardware with multiple cores, threads, etc. In most cases, serial programs run on modern computers "waste" potential computing power.

II. LITREATURE REVIEW

An easy way to comply with the conference paper The main challenge as computer architects is to deliver end-to-end performance growth at historical levels in the presence of technology discontinuities. We can address this challenge by focusing on power optimization at all levels [1].

Compared to DRAM, the new memories have two major differences, non-volatility and write overhead in terms of endurance, latency and power. The impact of new memory-aware software/hardware designs on program performance on a DRAM/SRAM hybrid memory [2]. Each system has large, shared semiconductor memories.

The models are validated using simulation. They can be utilized to quickly reduce the design space and study various trade-offs [3]. As DRAM faces scaling limit, several new memory technologies are considered as candidates for replacing or complementing DRAM main memory.

And SRAM Compared to DRAM, the new memories have two major differences, non-volatility and write overhead in terms of endurance, latency and power.the impact of new memory-aware software/hardware designs on program performance on a DRAM/SRAM hybrid memory [4].

III.PROBLEM IDENTIFICATION

The major issues involved in parallel computing architecture are:-

- The number of processing elements (PEs), computing power of each element and amount/organization of physical memory used .i.e the amount of computational resources are allocated to each processing element.
- One of the major issues involved is how data is shared between the processors.
- Parallel Processing Performance and Scalability Goals by minimizing parallelization overheads and balancing workload on processors thereby enhancing the scalability of performance on larger subsystems.

DOI 10.17148/IJARCCE.2016.5153

IV. PROPOSED METHODOLOGY

In many practical applications that demand a real time it is response, the computational work load in often fixed with a fixed problem size. As the number of processor increases in a parallel computer, the fixed load is distributed to more processor for parallel execution therefore; the main objective is to produce the results as soon as possible. In other words minimal turnaround time is the primary goal.

Speedup obtained for time-critical application is fixed load speedup.

Fixed Load Speedup

S = Time (the most efficient sequential algorithm) / Time (parallel algorithm)

Efficiency

E = S / N

With N is the number of processors

Selection

1. MIPS = (instructions/second)x 10-6
2. MFLOPS = (floating point ops/second)x 10-6
3. CPI = Average cycles per instruction
4. Throughput: number of results per second
5. Workload: W, number of Ops. Required to complete the program
6. Speed: W/TE
7. Speedup (S)= Te / Timprove
8. Efficiency (using P processors) = Speedup / P

The problem of optimally assigning the modules of a parallel program over the processors of a multiple-computer system is addressed. A sum-bottleneck path algorithm is developed that permits the efficient solution of many variants of this problem under some constraints on the structure of the partitions.

In particular, the following problems are solved optimally for a single-host, multiple-satellite system: partitioning multiple chain-structures parallel programs, multiple arbitrarily structured serial programs, and single-tree structured parallel programs. In addition, the problem of partitioning chain-structured parallel programs across chain-connected systems is solved under certain constraints. All solutions for parallel programs are equally applicable to pipelined programs

V. CONCLUSION

This current work presents a new approach which involved using of token memory. The token memory (TM) stores mainly the instructions which are transferred to basically reduce the overload on processing similar to accumulators or registers in conventional computers.

When there is The size of the TM is expected to be relatively small because the data values occupy space in the TM for a very short time. The small scale TM in our architecture makes it possible to reduce the complexity of the switch mechanism between functional units and memories, and the size of the control circuit.

Learning arises from the patterns of activation that

1. Extended circuitry
2. Best performance and heat less work
3. Faster services

REFERENCES

[1] J. Han et al., Mining Frequent Patterns without Candidate Generation: A Frequent- Pattern Tree Approach Data Mining and Knowledge Discovery.

[2] M. Hu, and B. Liu, Mining and Summarizing Customer Reviews, in: Proceedings of AC SIGKDD International Conference on Knowledge Discovery and Data Mining (KDD'04), USA, 2004, pp. 168 – 177.

[3] B. Pang, L. Lee, and S. Vaithyanathan, Sentiment Classification Using Machine Learning Techniques, in: Proceedings of the 2002 Conference on Empirical Methods in Natural Language Processing (EMNLP'02), USA, 2002, pp.79 – 86.

[4] B.Liu, M.Hu and J. Cheng, Opinion Observer - Analyzing and comparing opinions on the Web, in: Proceedings of the 14th International Conference on World Wide Web (WWW'05), Japan.

[5] Double Layer Security using Visual Cryptography & Transform Based Steganography,Pallavi B, Vishala I L,IJ of Research in Engineering & Technology (IJRET) ISSN:2319-1163,VOL-3,Spl Issue-03,May-2014.

[6] An Improved (8,8) Color Visual Cryptography Scheme using Floyd Error Diffusion,Anantha Kumar Kondra ,Smt U.V.Ratna Kumari ,IJ of Engineering Research & Application (IJERA) ISSN:2248-9622,VOL-2,Issue-5,Sep-Oct-2012.

DOI 10.17148/IJARCCE.2016.5153